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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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*Ex parte* LILY P. LOOI and MANOJ KHARE

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Appeal 2008-0622
Application 09/752,874[1]
Technology Center 2100

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Decided: July 28, 2008

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*Before* JOSEPH L. DIXON, JAY P. LUCAS, and CAROLYN D. THOMAS, *Administrative Patent Judges*.

LUCAS, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal from a final rejection of claims 1 to 7, and 9 to 26 under authority of 35 U.S.C. § 134. The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

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[1] Application filed December 29, 2000. The real party in interest is Intel Corporation.

Appellants' invention relates to a system and method for efficiently conveying interrupts from devices (e.g., keyboard, mouse, etc.) to processors that will process the interrupt, using a plurality of scalable node controllers connected to the processors and a scalability port switch conveying the interrupts to the node controllers. In the words of the Appellants:

> Figure 2 illustrates an interrupt delivery system 20 for a multi-node computer system in accordance with one embodiment of the present invention. Interrupt delivery system 20 includes a first SNC 22, which is coupled to processors 24a-d, and a second SNC 26, which is coupled to processors 28a-d. Both SNCs 22 and 26 are coupled to a SPS 30, which is in turn coupled to an IOH 32. IOH 32 is also coupled to a PCI 64-bit hub (P64H) 34, which supports a number of PCI devices 36a-d.
>
> If, for example, PCI device 36a requires servicing, it generates an interrupt request (IRQ), which is transmitted to P64H 34 through a side wire 37. After receiving the IRQ, an interrupt controller inside P64H 34 converts the IRQ into a write command and an ID 38 containing the destination information of the IRQ. ID 38 preferably includes a node address 40 and a processor address 42. The data is then transmitted to SPS 30 through IOH 32 (which will be detailed below) as a write command having an attribute equal to an interrupt and ID 38.
>
> Based on the node ID, SPS 30 will transmit the write command and its attribute to the correct SNC. The SPS accomplishes this task because it contains registers that stores the ID of the SNCs. Assuming that SNC 22 is identified by node address 40, SNC 22 will read processor address 42 to determine the correct destination processor.

(Spec. 5).

Claim 1 is exemplary:

1. An interrupt delivery system, comprising:

a first pair of scaleable node controllers, wherein each of said scaleable node controllers supports at least one microprocessor;

a first scalability port switch coupled to each of said scaleable node controllers, wherein said first scalability port switch is to receive an interrupt request, determine an address of one of said scaleable node controllers from said interrupt request and transmit said interrupt request to said one of said scaleable node controllers.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

| | | |
|---|---|---|
| Olarig | US 5,944,809 | Aug. 31, 1999 |
| Tavallaei | US 5,987,538 | Nov. 16, 1999 |
| Neal | US 6,119,191 | Sep. 12, 2000 |
| Arndt | US 6,189,065 B1 | Feb. 13, 2001 (filed Sep. 28, 1998) |

Intel, *MultiProcessor Specification*, Version 1.4, 2-2 to 3-16 (1997).

REJECTIONS

R1: Claims 1 to 3, 9 to 12, 16 to 21, and 25 to 26 stand rejected under 35 U.S.C. § 102(b) for being anticipated by Tavallaei.

R2: Claims 1 to 3, 9 to 12, 14 to 21, and 23 to 26 stand rejected under 35 U.S.C. § 102(b) for being anticipated by Olarig.

R3: Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) for being obvious over Tavallaei in view of Neal.

R4: Claims 6 and 7 stand rejected under 35 U.S.C. § 103(a) for being obvious over Tavallaei in view of Neal and further in view of Intel.

R5: Claims 13 and 22 stand rejected under 35 U.S.C. § 103(a) for being obvious over Tavallaei in view of Arndt.

R6: Claims 13 and 22 stand rejected under 35 U.S.C. § 103(a) for being obvious over Olarig in view of Arndt.

Appellants contend that the claimed subject matter is not anticipated by Tavallaei or Olarig, or rendered obvious by Tavallaei or Olarig in combination with Neal, Intel or Arndt, for failure of the references to teach the claimed limitations, as will be discussed below. The Examiner contends that each of the claims is properly rejected.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Brief and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this opinion. Arguments which Appellants could have made but chose not to make in the Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).[2]

[2] Appellants have not presented any substantive arguments directed separately to the patentability of the dependent claims or related claims in each group, except as will be noted in this opinion. In the absence of a separate argument with respect to those claims, they stand or fall with the

We affirm the rejections.

## ISSUE

The issue is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. §§ 102(b) and 103(a). The issue turns on whether the references disclose all of the claimed subject matter, when fairly interpreted by the Office.

## PRINCIPLES OF LAW

"In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.,* 432 F.3d 1368, 1375-76 (Fed. Cir. 2005) (citation omitted).

"Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) ("In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless

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representative independent claim. *See In re Young,* 927 F.2d 588, 590 (Fed. Cir. 1991).

of whether it also covers subject matter not in the prior art.") (internal citations omitted).

> Though understanding the claim language may be aided by the explanations contained in the written description, it is important not to import into a claim limitations that are not part of the claim. For example, a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment."

*Superguide Corp. v. DirecTV Enterprises, Inc*., 358 F.3d 870, 875 (Fed. Cir. 2004).

Shortly after the creation of this court, Judge Rich wrote that "[t]he descriptive part of the specification aids in ascertaining the scope and meaning of the claims inasmuch as the words of the claims must be based upon the description. The specification is, thus, the primary basis for construing the claims." *Standard Oil Co. v. Am. Cyanamid Co.*, 774 F.2d 448, 452 (Fed. Cir. 1985). "On numerous occasions since then, we have reaffirmed that point…" *Phillips v. AWH Corp*., 415 F.3d 1303, 1315 (Fed. Cir. 2005).

"[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.,* 415 F.3d at 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of

the effective filing date of the patent application." *Phillips v. AWH Corp.*, 415 F.3d at 1313 (Fed. Cir. 2005) (en banc).

ANALYSIS

From our review of the administrative record, we find that Examiner has presented a prima facie case for the rejections of Appellants' claims under 35 U.S.C. §§ 102(b), and 103(a). The prima facie case is presented on pages 3 to 12 of the Examiner's Answer. In opposition, Appellants present a number of arguments.

*Arguments with respect to rejections under 35 U.S.C. § 102(b) [R1] and [R2]*

[R1]

The Examiner has rejected claims 1 to 3, 9 to 12, 16 to 21, and 25 to 26 for being anticipated by Tavallaei. The Appellants' first argument contends that the Examiner has misconstrued the term Scaleable Node Controller (SNC). (Br., 4, middle). Examiner has read the Appellants' SNC on the advanced programmable interrupt controller (APIC) 14, which is shown in Figs. 1 and 2 of Tavallaei to direct the interrupt requests to the processors 12. The Appellants argue that a node controller performs a different function than an interrupt controller, and that an interrupt controller would not have suitable structure to perform the function of controlling a node of a multi-node system. (Br., 5, top).

Consistent with the teachings of *Phillips v. AWH Corp* (cited above), we start our analysis by reviewing whether the Examiner erred in interpreting the claimed term scaleable node controller. The Examiner has found, and we have likewise found, that the common meaning of node controller would encompass the function of an interrupt controller. Appellants agree on that point. (Br., 4, bottom). But Appellants say that a node controller has more. (Br., 5, top), and relies on "the common meaning" of node controller for that. We do not find that the Appellants have presented sufficient evidence, either in the Specification or on the record, for attributing more functions to the node controller in the context of these claims. The interrupt controller performs all of the functions required by the claims, even read in the context of the Specification. Statements that a node controller can perform more functions irrelevant to the claimed (and disclosed) subject matter do not obviate the anticipation of the claims by a functioning apparatus that does perform all the required/recited functions. (See *Atlas Powder Co. v. IRECO, Inc.* cited above.) In addition, the term "node controller" or "scaleable node controller" does seem to be a non-distinct and flexible claim term, upon review of various technical dictionaries. If Appellants cared to establish a set "term of art" for the purposes of this application (see *Phillips*, cited above), the Appellants had every opportunity to do so. If there were a well settled definition of node controller that excluded the APIC, the Appellants had every opportunity to

present evidence to that effect. However, on the record before us, we decline to find error in the Examiner's rejection on this point.

Appellants next contend that the Examiner has misconstrued the claim term "Scalability Port Switch" (SPS). The Examiner has read the Appellants' SPS on the "I/O APIC" #26 of Tavallaei, as shown in Figure 2 (see Answer, 3, middle), as the component #26 performs the same function as the claimed component in directing an interrupt request to the proper processor via the node controller. As the arguments are similar to those discussed in detail above, we will simply state that for the reasons expressed by the Examiner in the Answer (page 13, bottom) we do not find error in the rejection on this issue.

In the section of the Brief related to Tavallaei entitled the Theory of Inherency (Br., 8, bottom), Appellants with regard to claim 1 contend that Tavallaei fails to teach the claimed determining of an address to the SNC, and transmitting that address. The Examiner in the rejection points to Tavallaei at column 7, lines 7 to 9, and we further note that later in that column, at line 42, the addressing of the interrupt to the proper processor via the APIC (SNC) is performed. Later in Appellants' arguments in the Inherency section with respect to claims 11 and 20, Appellants argue that Tavallaei fails to teach the comparing of the priority of the interrupt request to the priority of the processor. As pointed out by the Examiner (Answer, 14, bottom), Tavallaei does teach comparison of the priorities, in (Col. 7, ll. 41 to 44). We do not find error in the rejection in regard to this argument.

[R2]

Examiner has rejected claims 1 to 3, 9 to 12, 14 to 21, and 23 to 26 for being anticipated by Olarig. Appellants present the same three arguments concerning misconstruing of the Scaleable Node Controller, misconstruing of the Scalability Port Switch, and the Inherency arguments (SNC address and priority of interrupts requests) as applied to Tavallaei in the arguments against anticipation by Olarig. The Examiner has presented his reasoning for the rejection over Olarig in the Answer on pages 15, 16 and the top of 17. In his response, the Examiner has presented the exact citations in the reference on which he is relying, and we do not find that Olarig is deficient in supplying the structure for the anticipation of the claims.

With regard to the arguments of the Appellants concerning the identity of the node controller and the interrupt controller, we adopt the arguments presented above with respect to Tavallaei but now applied to Olarig. The functions of the node controller with respect to this Specification are fully met by the APIC interrupt controllers described in Olarig. Alleged other functions that may be performable by a node controller are not relevant to obviating Olarig as an anticipatory reference.

*Arguments with respect to rejections*
*under 35 U.S.C. § 103(a) [R3], [R4], [R5] and [R6]*

The Examiner has rejected claims 4 and 5 for being obvious over Tavallaei in view of Neal. Claims 6 and 7 stand rejected over Tavallaei in

view of Neal and Intel. Appellants characterize the issue as, "[t]he Board should ask itself, would one of ordinary skill in the art as of December 29, 2000, without any knowledge of applicants' own invention, consider the ASIC 28 described by Neal to be an I/O hub?" (Br., 17, middle). The claim goes on to specify that the hub is coupled "between the peripheral component interconnect bus and the first scalability port switch . . .". In the Answer, the Examiner notes "[t]he specification discloses an input/output hub connected to a SPS 30 and P64H . . . an input/output hub functions as a component transmitting interrupt requests to a scalability port switch." In Figure 4 of Tavallaei, I/O chipset 28 [read on the hub] performs that connection. Neal is only used to demonstrate the use, in an analogous system, of a plurality of hubs, as required by a claim limitation. Intel clearly shows in Figure 2-2, page 2-3, a plurality of hubs, each performing its function in an expected manner. As all of the important components are indicated in the references, we do not find error in this rejection. [R3] [R4].

The Examiner has rejected claims 13 and 22 over Tavallaei in view of Arndt, [R4] and Olarig in view of Arndt [R5]. Appellants argue that the cited art does not teach the "scaleable node controller" nor the "scalability port switch" and thus a reference that merely teaches "redirecting an interrupt to a different processor" cannot render the claims obvious. (Br., 19, middle). The Examiner explains that the rejection is based on the combination of references, and the teachings of the SNC and SPS have been discussed. (Answer, 19, top). We agree.

## CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that the Examiner did not err in rejecting claims 1 to 7, and 9 to 26 as indicated above.

## DECISION

The Examiner's rejections [R1] to [R6] of claims 1 to 7 and 9 to 26 are Affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

rwk

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